What is claimed is:

# CLAIMS

1. A method for efficiently managing a set of data buffers accessible to first and second devices interconnected by a bus, the method comprising:

storing a set of free buffer descriptors in a buffer cache accessible to the first device, each free buffer descriptor referencing a respective data buffer available to store data;

determining whether the number of descriptors in the set of free buffer descriptors is greater than a predetermined threshold value; and

transferring, in response to the number of descriptors being greater than the predetermined threshold value, free buffer descriptors from the first device to the second device until the number of descriptors in the set of free buffer descriptors is less than the predetermined threshold value.

2. The method of claim 1, further comprising:

adjusting the number of free buffer descriptors stored in the buffer cache in accordance with a data path protocol implemented over the bus between the first and second devices.

3. The method of claim 1, further comprising:

storing at least one descriptor in the set of free buffer descriptors in a memory that is external to the first device; and

storing the remaining descriptors in the set of free buffer descriptors in the buffer cache located in a memory that is internal to the first device.

4. The method of claim 3, wherein the external memory is located in the second device.

5. The method of claim 3, further comprising:

transferring descriptors in the set of free buffer descriptors between the internal and external memories in a manner that is transparent to the second device.

6. The method of claim 5, further comprising:

transferring, in response to the number of free buffer descriptors in the buffer cache being greater than a maximum trigger threshold value, free buffer descriptors from the internal memory to the external memory until the number of descriptors in the buffer cache is less than or equal to a maximum target threshold value.

7. The method of claim 5, further comprising:

transferring, in response to the number of free buffer descriptors in the buffer cache being less than a minimum trigger threshold value, free buffer descriptors from the external memory to the internal memory until the number of descriptors in the buffer cache is greater than or equal to a minimum target threshold value.

8. The method of claim 1, further comprising:

transferring free buffer descriptors from the second device to the first device;

storing the free buffer descriptors transferred from the second device into the buffer cache.

9. The method of claim 8, wherein the step of transferring free buffer descriptors from the second device to the first device further comprises:

storing the free buffer descriptors transferred from the second device in a free-buffer first in, first out (FIFO) queue located in the first device.

10. The method of claim 8, wherein the step of transferring free buffer descriptors from the second device to the first device further comprises:

modifying the contents of the free buffer descriptors transferred from the second device to indicate that the transferred descriptors reference respective data buffers containing zero bytes of data.

11. The method of claim 1, wherein the bus is a split transaction bus.

12. A system configured to efficiently manage a set of data buffers, the system comprising:

a central processing unit (CPU);

a To-CPU direct memory access (DMA) engine configured to transfer data to the CPU for processing, the data being transferred to one or more data buffers in the set of data buffers;

a From-CPU DMA engine configured to retrieve processed data from one or more data buffers in the set of data buffers;

a buffer cache configured to store a set of free buffer descriptors, each free buffer descriptor in the set of free buffer descriptors referencing a respective data buffer available to store data;

a buffer manager configured to retrieve free buffer descriptors from the buffer cache and supply the retrieved free buffer descriptors to the To-CPU DMA engine, and further configured to receive free buffer descriptors from the From-CPU DMA engine and return the received free buffer descriptors to the buffer cache.

13. The system of claim 12, wherein the buffer manager is further configured to receive non-recycled descriptors from the From-CPU DMA engine and forward the non-recycled descriptors to the CPU.

14. The system of claim 12, wherein the buffer manager is further configured to transfer free buffer descriptors between first and second devices interconnected by a bus.

15. The system of claim 14, wherein the buffer manager transfers free buffer descriptors from the buffer cache located in the first device to an external memory resident in the second device.

16. The system of claim 14, wherein the bus is a split transaction bus.

17. An apparatus for efficiently managing a set of data buffers accessible to first and second devices interconnected by a bus, the apparatus comprising:

means for storing a set of free buffer descriptors in a buffer cache accessible to the first device, each free buffer descriptor referencing a respective data buffer available to store data;

means for determining whether the number of descriptors in the set of free buffer descriptors is greater than a predetermined threshold value; and

means for transferring, in response to the number of descriptors being greater than the predetermined threshold value, free buffer descriptors from the first device to the second device until the number of descriptors in the set of free buffer descriptors is less than the predetermined threshold value.

18. The apparatus of claim 17, further comprising:

means for adjusting the number of free buffer descriptors stored in the buffer cache in accordance with a data path protocol implemented over the bus between the first and second devices.

19. The apparatus of claim 17, further comprising:

means for storing at least one descriptor in the set of free buffer descriptors in a memory that is external to the first device; and

means for storing the remaining descriptors in the set of free buffer descriptors in the buffer cache located in a memory that is internal to the first device.

20. The apparatus of claim 19, wherein the external memory is located in the second device.

21. The apparatus of claim 19, further comprising:

means for transferring descriptors in the set of free buffer descriptors between the internal and external memories in a manner that is transparent to the second device.

22. The apparatus of claim 21, further comprising:

means for transferring, in response to the number of free buffer descriptors in the buffer cache being greater than a maximum trigger threshold value, free buffer descriptors from the internal memory to the external memory until the number of descriptors in the buffer cache is less than or equal to a maximum target threshold value.

23. The apparatus of claim 21, further comprising:

means for transferring, in response to the number of free buffer descriptors in the buffer cache being less than a minimum trigger threshold value, free buffer descriptors from the external memory to the internal memory until the number of descriptors in the buffer cache is greater than or equal to a minimum target threshold value.

24. A computer-readable media including instructions for execution by a processor, the instructions for a method of efficiently managing a set of data buffers accessible to first and second devices interconnected by a bus, the method comprising:

storing a set of free buffer descriptors in a buffer cache accessible to the first device, each free buffer descriptor referencing a respective data buffer available to store data;

determining whether the number of descriptors in the set of free buffer descriptors is greater than a predetermined threshold value; and

transferring, in response to the number of descriptors being greater than the predetermined threshold value, free buffer descriptors from the first device to the second device until the number of descriptors in the set of free buffer descriptors is less than the predetermined threshold value.